IN CLAIMS

32 (currently amended). A memory cell comprising:

an area defined by an intersection of a word line and a bit line;

an access device;

a memory element operatively coupled to the access device, the memory element comprising:

dielectric material having a pore therein, the pore being smaller than a photolithographic limit;

a first electrode disposed within the pore;

a memory material disposed over the first electrode; and

a second electrode disposed over the memory material; and

wherein ~~at least one of~~ the access device and the memory element ~~is~~are disposed wholly in the area.

33. (previously presented) The memory cell, as set forth in claim 32, wherein the access device comprises a diode.

34. (previously presented) The memory cell, as set forth in claim 33, wherein the diode comprises:

a layer of N doped polysilicon disposed adjacent a layer of P doped polysilicon.

35. (previously presented) The memory cell, as set forth in claim 32, wherein the first electrode is comprised of a plurality of layers.

36. (previously presented) The memory cell, as set forth in claim 32, wherein the first electrode is comprised of a plurality of materials.

37. (previously presented) The memory cell, as set forth in claim 32, wherein the first electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

38. (previously presented) The memory cell, as set forth in claim 32, wherein the second electrode is comprised of a plurality of layers.

39. (previously presented) The memory cell, as set forth in claim 32, wherein the second electrode is comprised of a plurality of materials.

40. (previously presented) The memory cell, as set forth in claim 32, wherein the second electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

41. (previously presented) The memory cell, as set forth in claim 32, wherein the memory material comprises structure changing material.

42. (previously presented) The memory cell, as set forth in claim 41, wherein the structure changing material comprises a material which changes between different states of crystallinity in response to electrical stimulus.

43. (previously presented) The memory cell, as set forth in claim 42, wherein each of the different states of crystallinity corresponds to a given resistance level.

44. (previously presented) The memory cell, as set forth in claim 32, wherein the memory material comprises a chalcogenide material.

45. (previously presented) The memory cell, as set forth in claim 32, wherein the memory material comprises a programmable resistive element.

46. (previously presented) The memory cell, as set forth in claim 45, wherein the programmable resistive element changes between different resistance levels in response to electrical stimulus.

47. (currently amended) A memory cell comprising:

an area defined by an intersection of a word line and a bit line;

an access device;

a memory element operatively coupled to the access device, the memory element comprising a memory material disposed between a first electrode and a second electrode; and

dielectric material having a pore therein, the pore being smaller than a photolithographic limit, wherein at least one of the first electrode, the memory material, and the second electrode is disposed within the pore; and

wherein ~~at least one of~~ the access device and the memory element ~~is~~are disposed wholly in the area.

48. (previously presented) The memory cell, as set forth in claim 47, wherein the access device comprises a diode.

49. (previously presented) The memory cell, as set forth in claim 48, wherein the diode comprises:

a layer of N doped polysilicon disposed adjacent a layer of P doped polysilicon.

50. (previously presented) The memory cell, as set forth in claim 47, wherein the first electrode is comprised of a plurality of layers.

51. (previously presented) The memory cell, as set forth in claim 47, wherein the first electrode is comprised of a plurality of materials.

52. (previously presented) The memory cell, as set forth in claim 47, wherein the first electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

53. (previously presented) The memory cell, as set forth in claim 47, wherein the second electrode is comprised of a plurality of layers.

54. (previously presented) The memory cell, as set forth in claim 47, wherein the second electrode is comprised of a plurality of materials.

55. (previously presented) The memory cell, as set forth in claim 47, wherein the second electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

56. (previously presented) The memory cell, as set forth in claim 47, wherein the memory material comprises structure changing material.

57. (previously presented) The memory cell, as set forth in claim 56, wherein the structure changing material comprises a material which changes between different states of crystallinity in response to electrical stimulus.

58. (previously presented) The memory cell, as set forth in claim 57, wherein each of the different states of crystallinity corresponds to a given resistance level.

59. (previously presented) The memory cell, as set forth in claim 47, wherein the memory material comprises a chalcogenide material.

60. (previously presented) The memory cell, as set forth in claim 47, wherein the memory material comprises a programmable resistive element.

61. (previously presented) The memory cell, as set forth in claim 60, wherein the programmable resistive element changes between different resistance levels in response to electrical stimulus.

62. (previously presented) An X-point memory cell comprising:

a first conductive line extending in a first direction;

a second conductive line extending in a second direction different than the first direction, the first conductive line and the second conductive line being spaced apart by a portion of a substrate, the second conductive line intersecting the first conductive line in an overlapping manner to form an area of intersection in the portion of the substrate;

an access device wholly disposed in the area of intersection, the access device being operatively coupled to one of the first conductive line and the second conductive line;

a memory element wholly disposed in the area of intersection, the memory element being operatively coupled to the access device, the memory element comprising a memory material disposed between a first electrode and a second electrode; and

dielectric material having a pore therein, the pore being smaller than a photolithographic limit and being wholly disposed in the area of intersection, wherein at least one of

the first electrode, the memory material, and the second electrode is disposed within the pore.

63. (previously presented) The memory cell, as set forth in claim 62, wherein the access device comprises a diode.

64. (previously presented) The memory cell, as set forth in claim 63, wherein the diode comprises:

a layer of N doped polysilicon disposed adjacent a layer of P doped polysilicon.

65. (previously presented) The memory cell, as set forth in claim 62, wherein the first electrode is comprised of a plurality of layers.

66. (previously presented) The memory cell, as set forth in claim 62, wherein the first electrode is comprised of a plurality of materials.

67. (previously presented) The memory cell, as set forth in claim 62, wherein the first electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

68. (previously presented) The memory cell, as set forth in claim 62, wherein the second electrode is comprised of a plurality of layers.

69. (previously presented) The memory cell, as set forth in claim 62, wherein the second electrode is comprised of a plurality of materials.

70. (previously presented) The memory cell, as set forth in claim 62, wherein the second electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

71. (previously presented) The memory cell, as set forth in claim 62, wherein the memory material comprises structure changing material.

72. (previously presented) The memory cell, as set forth in claim 71, wherein the structure changing material comprises a material which changes between different states of crystallinity in response to electrical stimulus.

73. (previously presented) The memory cell, as set forth in claim 72, wherein each of the different states of crystallinity corresponds to a given resistance level.

74. (previously presented) The memory cell, as set forth in claim 62, wherein the memory material comprises a chalcogenide material.

75. (previously presented) The memory cell, as set forth in claim 62, wherein the memory material comprises a programmable resistive element.

76. (previously presented) The memory cell, as set forth in claim 75, wherein the programmable resistive element changes between different resistance levels in response to electrical stimulus.

77. (previously presented) An X-point memory cell comprising:

a first conductive line extending in a first direction;

a second conductive line extending in a second direction different than the first direction, the first conductive line and the second conductive line being spaced apart by a portion of a substrate, the second conductive line intersecting the first conductive line in an overlapping manner to form an area of intersection in the portion of the substrate;

an access device wholly disposed in the area of intersection, the access device being operatively coupled to one of the first conductive line and the second conductive line; and

a memory element wholly disposed in the area of intersection, the memory element being operatively coupled to the access device, the memory element comprising a memory material disposed between a first electrode and a second electrode.

78. (previously presented) The memory cell, as set forth in claim 77, wherein the access device comprises a diode.

79. (previously presented) The memory cell, as set forth in claim 78, wherein the diode comprises:

a layer of N doped polysilicon disposed adjacent a layer of P doped polysilicon.

80. (previously presented) The memory cell, as set forth in claim 77, wherein the first electrode is comprised of a plurality of layers.

81. (previously presented) The memory cell, as set forth in claim 77, wherein the first electrode is comprised of a plurality of materials.

82. (previously presented) The memory cell, as set forth in claim 77, wherein the first electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

83. (previously presented) The memory cell, as set forth in claim 77, wherein the second electrode is comprised of a plurality of layers.

84. (previously presented) The memory cell, as set forth in claim 77, wherein the second electrode is comprised of a plurality of materials.

85. (previously presented) The memory cell, as set forth in claim 77, wherein the second electrode comprises:

a layer of carbon; and

a layer of titanium nitride disposed adjacent the layer of carbon.

86. (previously presented) The memory cell, as set forth in claim 77, wherein the memory material comprises structure changing material.

87. (previously presented) The memory cell, as set forth in claim 86, wherein the structure changing material comprises a material which changes between different states of crystallinity in response to electrical stimulus.

88. (previously presented) The memory cell, as set forth in claim 87, wherein each of the different states of crystallinity corresponds to a given resistance level.

89. (previously presented) The memory cell, as set forth in claim 77, wherein the memory material comprises a chalcogenide material.

90. (previously presented) The memory cell, as set forth in claim 77, wherein the memory material comprises a programmable resistive element.

91. (previously presented) The memory cell, as set forth in claim 90, wherein the programmable resistive element changes between different resistance levels in response to electrical stimulus.